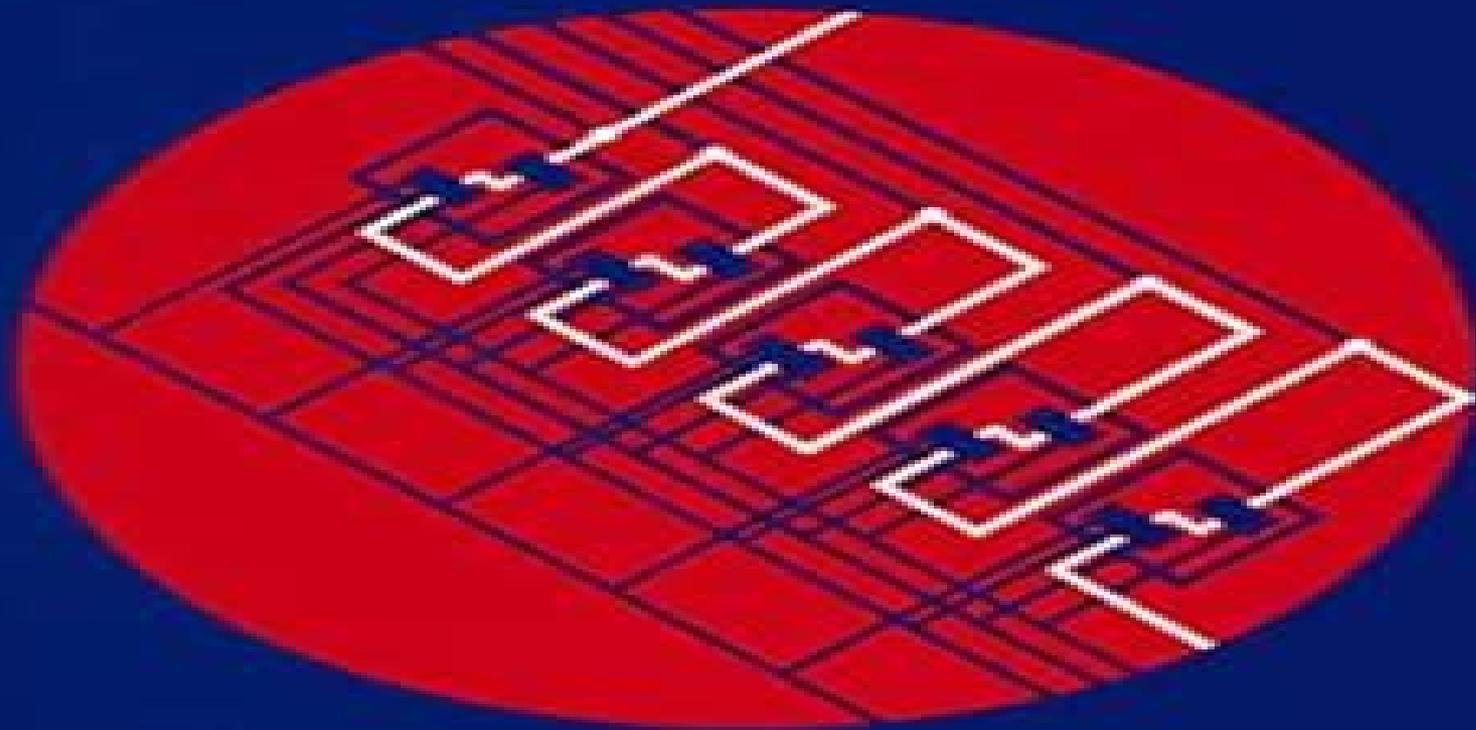




DESIGN OF TESTABLE LOGIC CIRCUITS

R. G. Bennetts



Design Of Testable Logic Circuits

Parag K. Lala



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Digital Circuit Testing and Testability Parag K. Lala,1997 An easy to use introduction to the practices and techniques in the field of digital circuit testing Lala writes in a user friendly and tutorial style making the book easy to read even for the newcomer to fault tolerant system design Each informative chapter is self contained with little or no previous knowledge of a topic assumed Extensive references follow each chapter [An Introduction to Logic Circuit Testing](#) Parag K.

Lala,2022-06-01 An Introduction to Logic Circuit Testing provides a detailed coverage of techniques for test generation and testable design of digital electronic circuits systems The material covered in the book should be sufficient for a course or part of a course in digital circuit testing for senior level undergraduate and first year graduate students in Electrical Engineering and Computer Science The book will also be a valuable resource for engineers working in the industry This book has four chapters Chapter 1 deals with various types of faults that may occur in very large scale integration VLSI based digital circuits Chapter 2 introduces the major concepts of all test generation techniques such as redundancy fault coverage sensitization and backtracking Chapter 3 introduces the key concepts of testability followed by some ad hoc design for testability rules that can be used to enhance testability of combinational circuits Chapter 4 deals with test generation and response evaluation techniques used in BIST built in self test schemes for VLSI chips Table of Contents Introduction Fault Detection in Logic Circuits Design for Testability Built in Self Test References **The Board Designer's Guide to Testable Logic**

Circuits Colin M. Maunder,1992 *Field-Coupled Nanocomputing* Neal G. Anderson,Sanjukta Bhanja,2014-05-31 Field coupled nanocomputing FCN paradigms offer fundamentally new approaches to digital information processing that do not utilize transistors or require charge transport Information transfer and computation are achieved in FCN via local field interactions between nanoscale building blocks that are organized in patterned arrays Several FCN paradigms are currently under active investigation including quantum dot cellular automata QCA molecular quantum cellular automata MQCA nanomagnetic logic NML and atomic quantum cellular automata AQCA Each of these paradigms has a number of unique features that make it attractive as a candidate for post CMOS nanocomputing and each faces critical challenges to realization This State of the Art Survey provides a snapshot of the current developments and novel research directions in the area of FCN The book is divided into five sections The first part Field Coupled Nanocomputing Paradigms provides valuable background information and perspectives on the QDCA MQCA NML and AQCA paradigms and their evolution The second section Circuits and Architectures addresses a wide variety of current research on FCN clocking strategies logic synthesis circuit design and test logic in memory hardware security and architecture The third section Modeling and Simulation considers the theoretical modeling and computer simulation of large FCN circuits as well as the use of simulations for gleaning physical insight into elementary FCN building blocks The fourth section Irreversibility and Dissipation considers the

dissipative consequences of irreversible information loss in FCN circuits their quantification and their connection to circuit structure The fifth section The Road Ahead Opportunities and Challenges includes an edited transcript of the panel discussion that concluded the FCN 13 workshop

Logic Testing and Design for Testability Hideo Fujiwara,1985-06 Design for testability techniques offer one approach toward alleviating this situation by adding enough extra circuitry to a circuit or chip to reduce the complexity of testing Today s computers must perform with increasing reliability which in turn depends on the problem of determining whether a circuit has been manufactured properly or behaves correctly However the greater circuit density of VLSI circuits and systems has made testing more difficult and costly This book notes that one solution is to develop faster and more efficient algorithms to generate test patterns or use design techniques to enhance testability that is design for testability Design for testability techniques offer one approach toward alleviating this situation by adding enough extra circuitry to a circuit or chip to reduce the complexity of testing Because the cost of hardware is decreasing as the cost of testing rises there is now a growing interest in these techniques for VLSI circuits The first half of the book focuses on the problem of testing test generation fault simulation and complexity of testing The second half takes up the problem of design for testability design techniques to minimize test application and or test generation cost scan design for sequential logic circuits compact testing built in testing and various design techniques for testable systems Logic Testing and Design for Testability is included in the Computer Systems Series edited by Herb Schwetman

VLSI Testing Stanley Leonard Hurst,1998 Hurst an editor at the Microelectronics Journal analyzes common problems that electronics engineers and circuit designers encounter while testing integrated circuits and the systems in which they are used and explains a variety of solutions available for overcoming them in both digital and mixed circuits Among his topics are faults in digital circuits generating a digital test pattern signatures and self tests structured design for testability testing structured digital circuits and microprocessors and financial aspects of testing The self contained reference is also suitable as a textbook in a formal course on the subject Annotation copyrighted by Book News Inc Portland OR

Design of Robustly Testable Combinational Logic Circuits International Business Machines Corporation. Research Division,S. Kundu,S. M. Reddy,Niraj K. Jha,1990

Reversible and DNA Computing Hafiz M. H. Babu,2020-11-09 Master the subjects of reversible computing and DNA computing with this expert volume Reversible and DNA Computing offers readers new ideas and technologies in the rapidly developing field of reversible computing World renowned researcher and author Hafiz Md Hasan Babu shows readers the fundamental concepts and ideas necessary to understand reversible computing including reversible circuits reversible fault tolerant circuits and reversible DNA circuits Reversible and DNA Computing contains a practical approach to understanding energy efficient DNA computing In addition to explaining the foundations of reversible circuits the book covers topics including Advanced logic design An introduction to the fundamentals of reversible computing Advanced reversible logic synthesis Reversible fault tolerance Fundamentals of DNA computing Reversible DNA logic synthesis DNA

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