Computer Applications Technology – Complete Guide

3G/4G ✔Ans - Generations of mobile phone technology that consists of high-tech infrastructure of networks and web 3G/4G- enabled handsets such as cellphones and smartphones.
4G is also known as LTE

AUP ✔Ans - -Acceptable User Policy
A policy which outlines the rights and responsibilities of its users, especially in networked environments.

Accessories ✔Ans - A number of useful programs come bundled with most operating systems. These are programs that are not specifically aimed at the core functioning of the operating systems.

ADSL ✔Ans - - Asymmetric Digital Subscriber Line
A permanent digital connection to the internet using a telephone line.

Adware ✔Ans - Software that downloads and bombards your computer with adverts that pop-up whenever you're connected to the internet.

Anti-virus software ✔Ans - Computer programs that scan computer files for viruses and eliminate them.

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web serial adder this repository contains structural code for serial adder the following individual components have been modeled and have been provided with their

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web to design such a circuit you are going to use the state diagram as the mode of describing the behavior of the circuit and then translate the state diagram into verilog code step

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web nov 1 2017   verilog code serial adder for n bits note that we dont have to mention n here module serial adder input clk reset clock and reset input a b cin note that cin is used for only first iteration output reg s cout note that s comes out at every clock cycle

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web fig circuit for moore type serial adder fsm the only difference between circuits of mealy and moore type fsm for serial adder is that in moore type fsm circuit output signal s is

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web sep 13 2021   step 1 concept full adder is a digital combinational circuit which is having three input a b and cin and two output sum and cout below truth table is drawn

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web file serial adder v is the master node the corresponding testbench is serial adder tb v to compile and visualise the waveforms using iverilog and gtkwave follow these steps