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Computer Architecture Complexity And Correctness

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Computer Architecture Complexity And Correctness:

Computer Architecture Silvia M. Mueller, Wolfgang J. Paul, 2013-11-11 Computer Architecture Complexity and Correctness develops at the gate level the complete design of a pipelined RISC processor with delayed branch forwarding hardware interlock precise maskable nested interrupts caches and a fully IEEE compliant floating point unit In contrast to other design approaches applied in practice and unlike other textbooks available the design presented here are modular clean and complete up to the construction of entire complex machines The authors systematically basing their approach on rigorous mathematical formalisms allows for rigorous correctness proofs accurate hardware costs determination and performance evaluation as well as generally speaking for coverage of a broad variety of relevant issues within a reasonable number of pages The book is written as a text for classes on computer architecture and related topics and will serve as a valuable source of reference for professionals in hardware design *Computer Architecture: Complexity And Correctness* Mueller, 2009-08-01

Correct Hardware Design and Verification Methods Tiziana Margaria, Tom F. Melham, 2001-08-27 This book constitutes the refereed proceedings of the 11th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods CHARME 2001 held in Livingston Scotland UK in September 2001 The 28 revised full papers and eight short papers presented together with two invited papers and one special paper were carefully reviewed and selected from 56 submissions The book offers topical sections on model checking clocking issues theorem proving with higher order logics hardware compilation tools component verification case studies algorithm verification and duration calculus *Correct Hardware Design and Verification Methods* Dominique Borrione, Wolfgang Paul, 2005-10-07 This book constitutes the refereed proceedings of the 13th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods CHARME 2005 held in Saarbrücken Germany in October 2005 The 21 revised full papers and 18 short papers presented together with 2 invited talks and one tutorial were carefully reviewed and selected from 79 submissions The papers are organized in topical sections on functional approaches to design description game solving approaches abstraction algorithms and techniques for speeding DD based verification real time and LTL model checking evaluation of SAT based tools model reduction and verification of memory hierarchy mechanisms *Correct Hardware Design and Verification Methods* Daniel Geist, Enrico Tronci, 2003-10-10 This book constitutes the refereed proceedings of the 12th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods CHARME 2003 held in L'Aquila Italy in October 2003 The 24 revised full papers and 8 short papers presented were carefully reviewed and selected from 65 submissions The papers are organized in topical sections on software verification automata based methods processor verification specification methods theorem proving bounded model checking and model checking and applications

Parallel Systems And Algorithms: Pasa '96 - Proceedings Of The 4th Workshop Ernst W Mayr, Frank Hopfeld, E Maehle, 1997-02-20 The PASA Workshops aim to build a bridge between theory and practice in the area of parallel

systems and algorithms Practical problems which require theoretical investigations as well as the applicability of theoretical approaches and results to practice are discussed A particularly important aspect is the communication and exchange of experiences between various groups working in various areas of parallel computing e g computer science electrical engineering physics and mathematics This volume discusses many aspects of parallel computing from a theoretical as well as a practice oriented point of view It shows that there are a number of promising approaches for the application of formal methods to the solution of practical problems in the area of parallel systems and algorithms *Proceedings of the 4th Workshop on PASA '96, Parallel Systems & Algorithms, Research Center Jülich, Germany, 10-12 April 1996* Workshop on PASA '96 1996, Research Center Jülich, Ernst W. Mayr, 1997 The PASA Workshops aim to build a bridge between theory and practice in the area of parallel systems and algorithms Practical problems which require theoretical investigations as well as the applicability of theoretical approaches and results to practice are discussed A particularly important aspect is the communication and exchange of experiences between various groups working in various areas of parallel computing e g computer science electrical engineering physics and mathematics This volume discusses many aspects of parallel computing from a theoretical as well as a practice oriented point of view It shows that there are a number of promising approaches for the application of formal methods to the solution of practical problems in the area of parallel systems and algorithms

Publisher's website *Formal Methods and Software Engineering*, 2003 **Proceedings of the ... ACM Great Lakes Symposium on VLSI**, 2004 *Proceedings of the Fourth Israel Symposium on Theory of Computing and Systems*, 1996 This volume contains a selection of 29 papers presented at the Fourth Israeli Symposium on the theory of Computing and Systems held in Jerusalem in June of 1996 Topics include the Borowsky Gafni simulation algorithm arrangements of curves and surfaces in computational geometry advances in optical *Proceedings of the ... International Workshop on Formal Methods for Industrial Critical Systems*, 2005 *GLSVLSI '04*, 2004 **American Book Publishing Record** R.R. Bowker Company, 1978 **From HDL Descriptions to Guaranteed Correct Circuit Designs** Dominique Borrione, 1987 Hardbound The objective of this book is to bring together the knowledge of developers and users of design automation tools and compare the methods and algorithms by which correct circuit designs may be obtained from initial descriptions and specifications written in an appropriate hardware description language HDL In order to achieve the goal of designing correct circuits two main directions of research are currently being pursued formal verification of a possibly manual design and automatic synthesis Both approaches require that a high level specification of the circuit be given in a formal language and an underlying model of hardware behaviour is necessary to allow for symbolic translations that preserve or verify some notion of correctness Hardware models formal proof of correctness and synthesis are therefore the three key elements making up this volume **The British National Bibliography** Arthur James Wells, 2000 *Computer Sciences Technical Report*, 2002 *SIAM Journal on Computing* Society for Industrial and Applied Mathematics, 1997 **Pascal for**

Engineers David T. Barnard, David B. Skillicorn, 1988 **Proceedings ISAI/IFIS ...**, 1996 *Catalogs of Courses*
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