

# The **PAPRICA** Massively Parallel Processor\*

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## Abstract

*This paper describes a complete 5-year project, starting from its theoretical basis up to the hardware and software system implementation, and to the description of its future evolution.*

*The main goal of the project is to develop a subsystem that operates as a processing unit attached to a standard workstation and in perspective as a low-cost low-sized specialized embedded system devoted to low level image analysis and cellular neural networks emulation. The architecture has been extensively used for basic low level image analysis tasks up to optical flow computation and feature tracking, showing encouraging performances even in the first prototype version.*

## 1 Introduction

The PAPRICA system [5, 11] (an acronym for Parallel Processor for Image Checking and Analysis) described in this paper and shown in fig. 1 has the main characteristics of a conventional mesh-connected SIMD array but it has been specialized to the following objectives:

- to directly support a computational paradigm based on mathematical morphology [16] also on data structures larger than the physical size of the machine;
- to support hierarchical non-mesh data structures;
- to provide a low-cost experimental tool for research in the fields of image processing, VLSI design automation, and neural algorithms.

The kernel of the system is a bidimensional mesh of single-bit Processing Elements (PE) with a direct 8-neighborhood [7]. The instruction set can be described in terms of mathematical morphology operators [16], augmented with logical operations. Control flow operations are defined over the entire SIMD mesh, and

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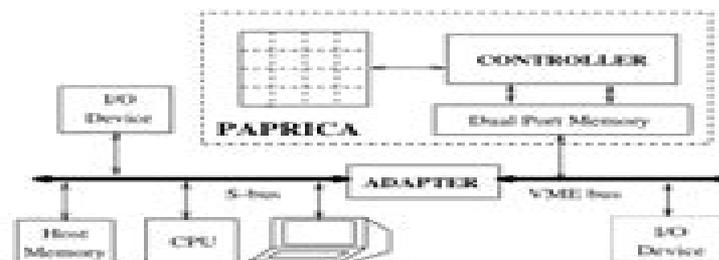


Figure 1: The complete system

hardware mechanisms are provided for the virtualization of the operation of the physically limited array over a large bidimensional data structure stored in a linearly addressable memory. An additional mechanism allows to map more complex hierarchical data structures on the same bidimensional processing grid.

The PAPRICA system has been designed to operate as a coprocessor of a general purpose host workstation. Data and instructions are transferred to and from the host through a dual port memory connected to a standard VME bus, while processing proceeds concurrently with the host activities.

The current PAPRICA implementation is based on a number of custom integrated circuits, which have been designed with a particular emphasis on global project management issues such as cost and development time. For this reason conservative design and engineering choices have often been taken leading to performance limitations both in terms of processing speed and in the number of available PEs.

The original target of the PAPRICA system is the acceleration of tasks related to the design and verification of IC layouts and masks. Nevertheless the generality of the mathematical morphology computational paradigm allows an efficient use of the architecture

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